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Design of a High Frequency Stable Oscillator with Tunable Frequency using Field Programmable CMOS Current Conveyor

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Abstract
Design of a programmable frequency oscillator design using field programmable, analog, CMOS current conveyor has been presented; further, a design methodology to introduce on-chip /field programmability into the second generation current controlled current conveyor circuit (CCCII) is explained. To make the CCCII CMOS design programmable, a floating-gate transistor synapse is introduced to replace the MOSFETs in the design. The charge at the floating-gate can be programmed after fabrication, based on Hot-e-injection and Fowler-Nordheim tunneling techniques. This programming charge at floating-gate results in threshold voltage variation in such floating-gate (FG) MOSFETs, which in turn can modifies circuit specifications after fabrication. The high frequency small signal analysis of the design has been discussed and specifications of the design are derived in terms of threshold voltages of the respective FG-MOSFETs. To achieve CCCII circuit's AC and DC characteristics and to obtain programmable oscillations, the programmable CCCII and oscillator circuit using programmable CCCII, are simulated using BSIM3 level49 MOSFET models in T-Spice 0.35µm CMOS process. The simulated results show 13bit programming precision in current gain, 3dB bandwidth, input impedance, output impedance and dc offsets with respect to threshold voltage of respective FG-MOSFETs. Moreover on employing CCCII design with programmable current gain (about 0.91258- 1.2138) in an oscillator design with minimum passive components, variable amplitude oscillations can be generated.

1. Introduction

Over the last two decades, second generation current controlled current conveyor (CCCII) due to their higher bandwidth, greater linearity, larger dynamic range, simpler circuitry, lower power consumption and less chip area than the classical op-amps, are gaining popularity in analog IC design [1]-[4]. CMOS CCCII design consists of four symmetric current mirrors and a mixed translinear loop with one low impedance input (controlled by bias current), one high impedance input, one high impedance output, a suitable element for both voltage-mode and current-mode circuits [5,6]. The design has an advantage that its intrinsic resistor can be controlled by biasing current which allows the implementation of numerous electronically adjustable functions. It can be elegantly applied to a variety of analog circuit design problems like Lossless Inductance, Floating Admittance, Super capacitor, Dual I/P integrator and differentiator, band pass filters, Voltage controlled oscillator, Sinusoidal oscillator, Balanced Integrator, CCCII with Negative resistance, Universal Filter, High frequency Oscillator. Of late, various high frequency sinusoidal oscillators using CCCII have been designed [6, 7, 8 and 9]. However we would like to introduce field programmability in high frequency oscillator [6] using our proposed field programmable CMOS CCCII design. Hence the paper first illustrate the programmable CCCII, its basic circuit, derived equations of its characteristics with respect to threshold voltage of respective transistors using high frequency small signal equivalent model and simulation results demonstrating a design methodology. Derived design methodology for CCCII design illustrate that for programming a specification what all floating-gate transistors need to be programmed and what fashion. It shows that the CCCII specifications can adapt with high precision to any desired value by field user. Then, later in the paper, oscillator using our proposed CCCII is described and its simulation results show programmable output oscillations with programming gain of CCCII.

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2. Field Programmable Analog CMOS CCCII

The basic design of CMOS second generation current controlled current conveyor, CCCII, is being simulated using BSIM3 level49 MOSFET models in T-Spice 0.35µm CMOS process with basic circuit configuration verifying its basic functionality while all the transistors in the design are replaced by FGMOS. Where Floating-gate MOS transistors are conventional MOS transistors wherein memory is stored in the form of charge trapped on floating-gate, affecting its threshold voltage. Two antagonistic quantum mechanical transfer processes, viz. injection and tunneling, alter the trapped charge on a floating gate. As these processes can occur during normal operation (indirect programming [10]), it leads additional attributes to the FGMOS transistors such as non volatile analog memory storage on floating-gate, locally computed bidirectional memory updates and memory modification
during normal transistor operation. Secondly the design's specifications or characteristics are being derived with the

help of its high frequency small signal equivalent model in terms of respective FGMOS threshold voltages. Next with the help of iterative simulation results and sensitivity analysis of each characteristic with respect to threshold voltages, a design methodology is being designed, which shows which FGMOS need to be programmed after fabrication for which design characteristics.

2.1 Analyze CMOS CCCII circuit design

Second generation current controlled current conveyor (CCCII) is a three terminal device with a terminal for biasing current. With low magnitude input bias current i_b (t), the mixed translinear loop forces the drain current of its each transistor equal to I_b. This consequently gives $V_x(t)=V_y(t)$. And hence, this equivalent voltage follower presents at port X a small signal intrinsic resistor R_x that is inversely proportional to the square root of the bias current I_b [2]. The two complementary current mirrors allows to duplicate on port Z the input current at X, then $i_z(t)=i_x(t)$. First, the design with basic sizing and biasing condition are analysed to achieve design functionality. The simulation plots of its characteristic such as current gain is presented in figure 2.

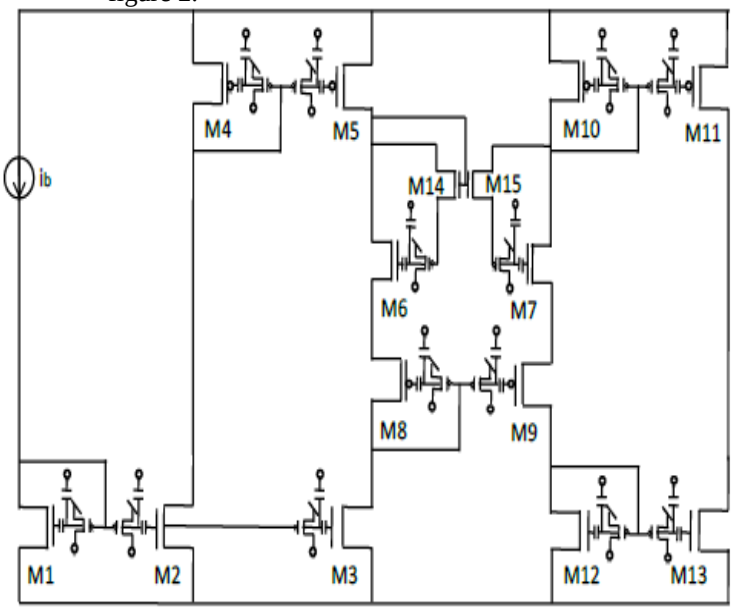

Fig.1 Proposed CMOS CCCII Design employing programmable FGMOSs

2.2 Derive Characteristics using its Equivalent High Frequency Small signal

The CCCII design is operated at high frequency. So to evaluate and derive design characteristics, high frequency small signal equivalent model is developed. The circuit consists of four current mirrors and a mixed translinear loop (as demonstrated in Figure 1). In translinear loop as gate-to-source voltage of transistor M6 and M8 are equal, drain currents of M6 and M8 can be considered equal. Hence on applying KCL at node 1, 2, X and Y, intrinsic resistance R_x, voltage gain (V_x/V_y), and current gain i_z (t)/i_x(t) are derived, respectively. Resistance R_x, using Thevinen theorem at port X, is given by:

$$R_X = \frac{1}{g_{m7}+g_{m9}} \quad (1)$$

Transconductances in equation 1 can be expressed in terms of square root of their respective saturation drain currents:

$$g_m = \frac{k_n' W/L}{2}\left(\sqrt{\frac{I_d}{k_n'/2W/L}}\right) \quad (2)$$

However, the currents id7 and id9 can be expressed in terms of bias current of the design, Ib. Hence, on substituting values of gm7 and gm9 in equation (1) in terms of their respective currents id7 and id9, which in turn can be written in terms of bias current Ib, expression of intrinsic impedance Rx proves that it is indirectly proportional to the square root of the bias current Ib.The voltage gain (Vx/Vy) across port X and Y in the design is expressed as:

$$A_v = \frac{(s(C_{gs6}+C_{gs7})+g_{m6}+g_{m7})(sC_{gd2}-g_{m2})(sC_{gd5}+g_{m5})}{(g_{m7}+sC_{gs7})(sC_{gd2}+g_{ds2})(sC_{gd5}+g_{ds5})}\frac{V_b}{V_Y} - \frac{(g_{m6}+sC_{gs6})}{(sC_{gs7}+g_{m7})} \quad (3)$$

where, Vb is the voltage across the bias current Ib of the circuit. Moreover, current gain Ai =iz(t)/ix(t), assuming id6 = id7 = id8 and id9 = id7 + ix , is expressed as:

$$A_i = \frac{(sC_{gd5}+g_{m5})(sC_{gd2}-g_{m2})}{(s(C_{gd5}+C_{gs5}+C_{gs4})-g_{m4})(s(C_{gs1}+C_{gs2}+C_{gd2})+g_{m1})}\frac{I_b}{i_x}$$

$$\left[\frac{sC_{gd11}+g_{m11}}{(s(C_{gd11}+C_{gs10}+C_{g11})-g_{m10}} - \frac{sC_{gd18}-g_{m18}}{(s(C_{gs12}+C_{gs18}+C_{gd18})+g_{m12}}\right] - \frac{sC_{gd18}-g_{m18}}{s(C_{gd18}+C_{gs18}+C_{gs12})+g_{m12}} \quad (4)$$

The current gain, voltage gain and the values of poles in current gain and voltage gain and -3db bandwidth are mentioned in Table I.

Output impedance at port Z from small signal equivalent circuit of the CCCII design is being derived as:

$$R_{out} = \frac{1}{(g_{ds2}+g_{ds8}+g_{ds5}+g_{ds7}+g_{ds9}+g_{ds11}+g_{ds18})+ s(C_{gd2}+C_{gd8}+C_{gd5}C_{gd7}+C_{gd9}+C_{gd11}+C_{gd18})} \quad (5)$$

Moreover, DC offsets, output offset voltage at X and output offset current at Z can be expressed by neglecting all parasitic capacitances in the expression (3) and (4), with no input voltage Vy or input current ix(t), respectively. Hence the output offset voltage at X is given by:

$$V_{offset} \cong -g_{m2}g_{m5}(g_{m6}+g_{m7})V_b \quad (6)$$

And output offset current at Z is given by:

$$I_{offset} \cong \frac{g_{m5}g_{m2}}{g_{m1}g_{m4}}\left[\frac{g_{m13}}{g_{m12}} - \frac{g_{m11}}{g_{m10}}\right] I_b \quad (7)$$

Therefore characteristics of the design have been derived in terms of small signal parameters of the transistor operated at high frequencies (conductance's and parasitic capacitances). However these parameters can be replaced in terms of threshold voltage as gm, the transconductance is expressed by equation (2). Hence all derived characteristics are expressed in terms of threshold
voltages of respective FGMOSs. Now sensitivity of each specification with respect to respective FGMOS's threshold voltage is being derived and iterative simulation results can lead us to a design methodology for on-chip programming of these characteristics. Figure 3 and 4 demonstrate the variation of current gain and voltage gain with programmable FGMOS respectively. Similarly all characteristics show variation with programming respective FGMOSs (about 13bit of programming resolution as claimed in [11]).

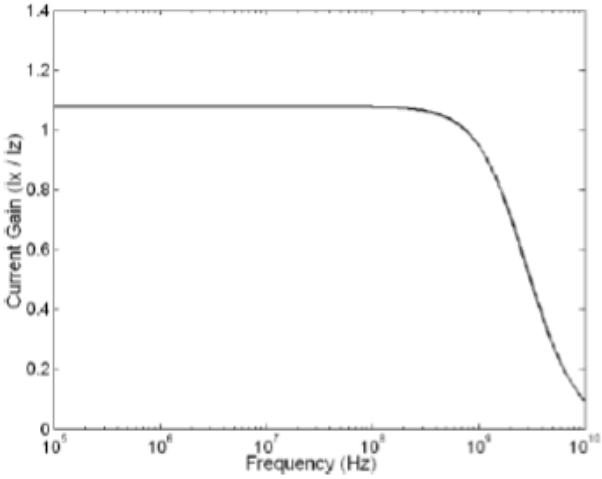

Fig.2 Frequency response of Current gain of CMOS CCCII design with basic circuit configuration

2.3 Proposed Design Topology for designing CCCII

The programming of all characteristics with each corresponding FGMOS is verified with simulations and most sensitive pairs of characteristic and FGMOS is characterized. The most sensitive pairs are:
Voltage Gain: Vt8
Current Gain: Vt11
Intrinsic Impedance: Vt6 or Vt7
Output Impedance: Vt13
However with variation in Vt's of these FGMOS of the sensitive pairs, rest of the specification also get affected. Thus while maintaining the most sensitive pair, the change in rest of the characteristics needs to be compensated. Like current gain is most sensitive to Vt11 while compensating rest of the characteristics (Rout) using other FGMOS Vt programming, i.e., with Vt13. Programming range of Ai obtain is about from 0.91258 to 1.2138 with 13bit of precision in programming. Hence an analog i.e. continuous, on-chip programming of gain can be attained.

Table 1 Main Characteristics of CCCII design at bias current, Ib =800μA and biasing voltages= ±2v

AC characteristics	
Current Gain α_o	1.079
-3dB bandwidth for α_s	4.7GHz
Voltage Gain β_o	0.559
-3dB bandwidth for β_s	5.24GHz
Intrinsic resistance R_x	26.12kΩ
Output resistance	843.29kΩ

DC characteristics	
Output offset voltage at X	35mV
Output offset current at Z	350pA
Total dissipation	1.509mW

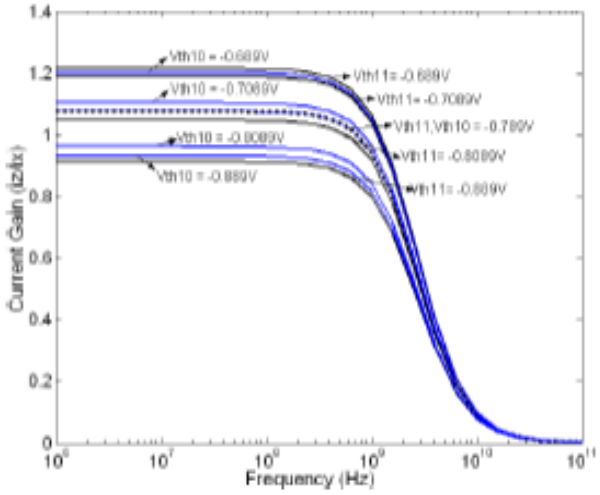

Fig 3: Variation of Current gain with change in threshold or programming of M10&M11 floating-gate transistor

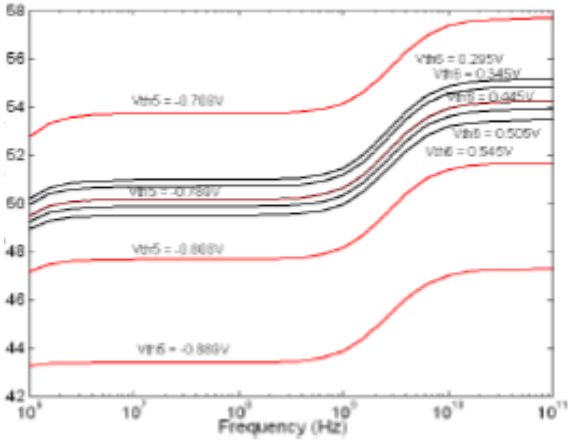

Fig.4 Variation of Voltage gain with change in threshold or programming of M5 and M6 floating-gate transistors

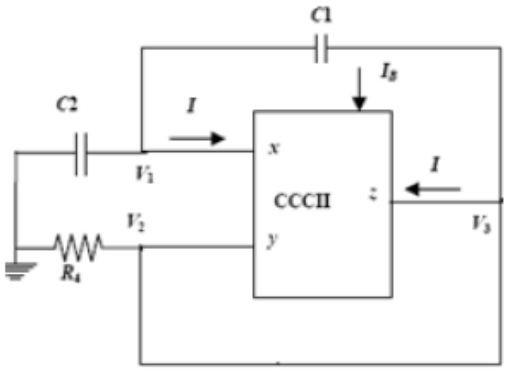

Fig. 5 Simplified circuit schematics of the CCCII based Oscillator. In our proposed design we employ programmable CCCII aforementioned to generate programmable oscillations.

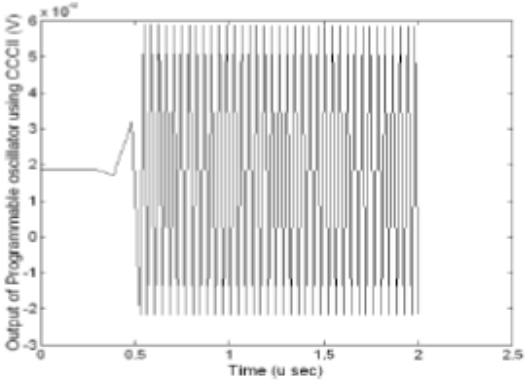

Fig.6 Output Wave of Oscillator using CCCII. The operating frequency is about 13.16 MHz with Ib=800µA, Vdd/Vss=± 1.5v, C1 & C2= 1pF &20fF, R1=1k.

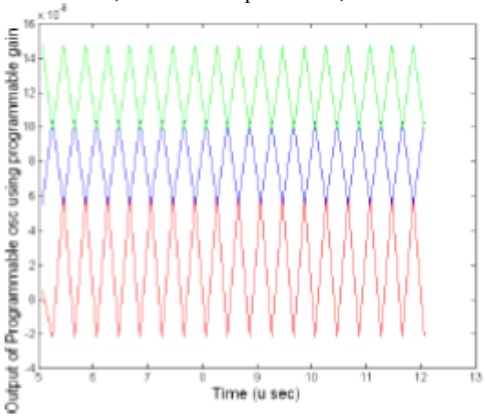

Fig.7 Output with Programmable Amplitude with CCCII current gain on-chip programming. Output (Red) corresponds to CCCII gain=1.0769, blue corresponds to gain=1.1886 and green corresponds to gain=1.2138.

3. Field Programmable Oscillator Using CCCII

The high frequency oscillator design using CCCII with minimum passive components design [6] is simulated using BSIM3 level49 MOSFET models in T-Spice 0.35µm CMOS process, as shown in Figure 5. The CCCII in the design is being replaced by our proposed on-chip programmable CCCII. Simulated results are being demonstrated in Figure 6 and Figure 7.

4. Conclusion

The design methodology for proposed programmable CMOS CCCII design is designed which illustrate the on-chip programming steps to generate accurate and optimized programming of CCCII specifications. This on-chip programmable CCCII design is in turn being used to generate programmable oscillations (programmable amplitude) in the high frequency oscillator design [6]. Therefore an analog, field programmable, high frequency oscillator is being proposed which can produce highly precise (13-bit resolution [11]), field programmable oscillations.

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